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DCRC Testing & Calibration Procedures

@Texas A&M University

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Terms used in this talk

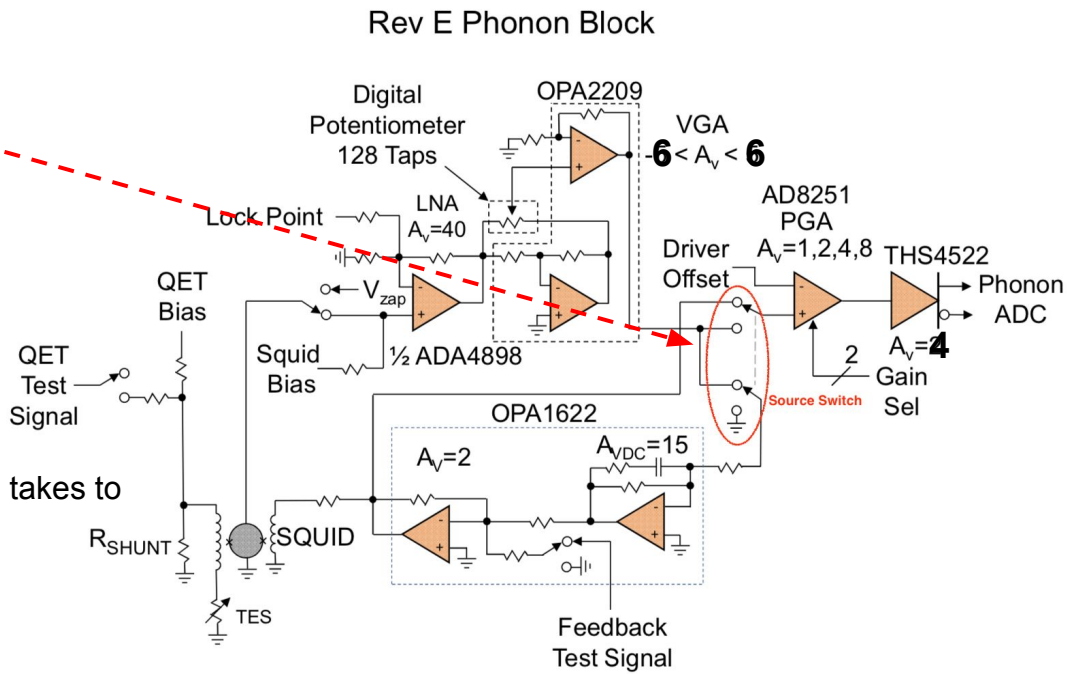
Source Switch:
The switch between Feedback and PreAmp mode.
FeedBack Mode: Source Switch Up
PreAmp Mode: Source Switch Down *

Feedback mode: closed loop
Preamp mode: open loop

InG: Input Gain
DrG: Driver Gain

Rise/Fall Time: The time one DCRC charge channel takes to change the offset from one to another.

FIR: Finite impulse response



* The whole point is that you can break the feedback loop

Outline

1. Motivation
2. Overview of the documentation
3. Test Stand
4. Tests and Calibration
   - 4.0 Power-on Test and PowerUp Test
   - 4.1 Noise Test
   - 4.2 Phonon Test
   - 4.3 Charge Test
   - 4.4 Hybrid Readout Test
   - 4.5 Calibration and DAQ Validating
5. Proposal
6. Conclusion
7. Appendix (railed trace, bad PSD, more details about calibration)

1. Motivation

We have developed a set of testing and calibration procedures for the DCRC RevE/Prod. (New tests will be added for Prod if there are new features)

Question:

- *Is the testing and calibration procedure good enough? Are DCRCs ready to use If they pass the tests?*

In this talk we will present procedure and results from our testing and calibration on RevE/Prod Boards. If there are no requests, we will consider these the official procedures for validating the RevE/Prod DCRC boards.

2. Overview of Documentation

- Homepage for DCRC on Confluence
  - https://confluence.slac.stanford.edu/pages/viewpage.action?spaceKey=CDMS&title=1.5.2+Detector+Control+and+Readout+Card
- Webpages for DCRC Testing and Calibration at TAMU
  - Homepage for DCRC Testing and Calibration at TAMU
  - DCRC RevE/Prod Testing and Calibration Instructions
  - Testing and Calibration Results (RevE, Prod)
  - Git Repository (PowerUp Test, Testbench)*
  - Technical Attachments to Testing and Calibration
- Firmware Versions to be used
  - MicroController Version: 2.09 (as of Feb 2020)
  - Big FPGA Version: 21f5a28 (as of Sep 2020)
  - Small FPGA Version: 0xb83a (as of Aug 2020)

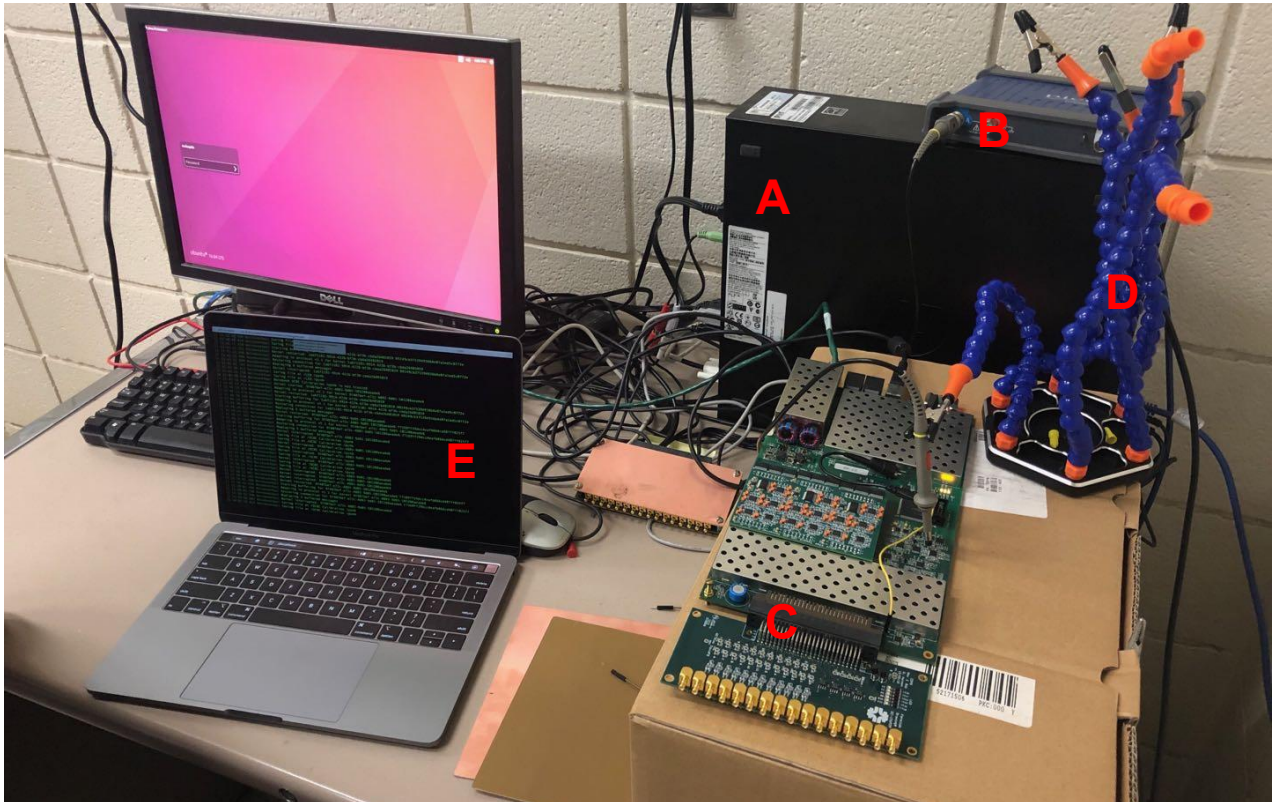
* ‘PowerUp Test’ is basic testing without external signal. ‘Testbench’ is other advanced testing items and those using external signals.

3. Test Stand

Two Test Stands @ TAMU

Each has:

- (A)PC
- (B)Picoscope
- (C)DCRC+miniBob
- (D)Helping hands
- (E)Laptop



4. Tests and Calibration - Overview

Procedures (Types of Tests and Calibrations)

1. Power-on tests (smoke and LED light) and PowerUp Test(13 Basic checks without an external signal generator. See 4.0.1 PowerUp Test - Overview.)
2. Noise Tests (trace, RMS, PSD)
3. Phonon Tests (Channel 0-11, Source Switch, InG&DrG, Trigger, Transfer Function)
4. Charge Tests (Channel 12-15, Offsets DACs, Trigger)
5. Hybrid Readout Test
6. Calibration and DAQ Validating

Decisions (Three types of checks for decision making.)

1. Basic Check, e.g. check if LED turn on
2. Visual Check, e.g. check the shape of the signal to see if it looks typical
3. Quantitative Check, e.g. check linearity of DrG and InG in preamp mode, check the calibration constants

Outputs (Other things produced along the way)

1. Calibration Constants
2. Data Plots (e.g. traces, PSD, transfer function, FIR output)
3. Test Result Summaries (e.g. features far different from typical results)

4. Tests and Calibration

4.0 Power-on Test and PowerUp Test

- 4.0.0 Power-on tests (smoke test, LED lights)
- 4.0.1 PowerUp Test (DCRC info, firmware, Trigger, Inversion, Readback)

4.1 Noise Tests (traces, RMS, PSDs)

4.2 Phonon Tests (Source Switch, InG&DrG, Trigger, Transfer Function)

4.3 Charge Tests (Offset DACs, Trigger)

4.4 Hybrid Readout Test

4.5 Calibration and DAQ Validating

4.0.0 Power-on Tests - Smoke Test and LED Check

Goal: Check there is no critical hardware issues.

Procedure: Power-on Test is the very first test, when a DCRC board arrives at TAMU. Power on the DCRC.

Decision Making

Good: no smoke, 5 LED lights are on.

Bad: 1) Board smokes, maybe somewhere shorted. 2) One or more of the lights don't turn on after initialization.

4.0.1 PowerUp Test - Overview

Goal: Basic checks (not completely in order of test code) on a DCRC without an external signal generator. It is also intended to be used in test facilities when they receive a new DCRC, if there is a power outage or you see some problems with the board and suspect something is wrong with the firmware. Here is the list of all testing item goal, as same order as Procedure and Decision Making.

1. DCRC Information(Serial Number, FPGA, CPLD, and Microcontroller version number) is correct/up-to-date.
2. Test Counter (0x30&0x31) works. Asynchronous address/data bus between the FPGA and microcontroller is good.
3. SDRAM works as it is designed.
4. Memory doesn't change while ADC disabled.
5. Low noise on all channel traces and offsets under control (no railed issue).
6. Phonon channels can be triggered.
7. The trigger amplitudes match trigger simulation amplitudes.
8. No phonon channel inversion.
9. Charge channels' offsets changes properly under commands.
10. Charge pulse injector mapping is correct
11. Charge channels can be triggered.
12. Random trigger works.
13. ALL read-and-write registers are both readable and writable.

Procedure:

1. **DCRC Information**: Connect to the DCRC, directly read out Serial Number, FPGA and Microcontroller version number, and print them out in the testing code.
2. **FPGA and microcontroller address/data Test**: Test the asynchronous address/data bus between the FPGA and microcontroller.

4.0.1 PowerUp Test - Overview (contd)

3. **SDRAM Test**: Test the interface between FPGA by and SDRAM by writing to a specific memory location and read back the memory.
4. **ADC Readout Test**: After ADC disabled, we read out the same trace twice and compare all the adc values
5. **Noise Traces Check:** See 4.1 Noise Test in this talk.
6. **Phonon Trigger Test**: Set the DCRC internal signal generator(Test Signal) to send the same square wave signal to all 12 phonon channels. If trigger gets fired, the traces(subtract the baselines) will be plotted. Visual Check.
7. **Trigger and Trigger Simulation Amplitudes Comparison:** Comparing Trigger and Trigger Simulation amplitudes for a long square trace where we get 255 trigger. (maximum number of trigger that FIFO can hold). Visual and quantitative check
8. **Phonon Inversion Check**: Set the DCRC internal signal generator(Test Signal) to send the same sine wave signal to all 12 phonon channels, read out from ADC simultaneously and plot the traces(subtract the baselines). Visual Check
9. **Charge Offset**: (4.3.0 Offset DAC Check)
10. **Charge Pulse Injector Mapping:** Send a pulse through the internal signal generator and plots the channels' outputs to verify it comes out the right channel. Visual check.
11. **Charge Trigger Test:**(4.3.1 Trigger Test w/ DCRC pulser)
12. **Random Trigger Test**: Randomly turns on the trigger to compare with expected background.
13. **Readback Test**: Initialize the DCRC board, read out the current values of ALL read-and-write registers. Then write a new value back into these registers and read out again. The new value will be compared to the old value, which is done by code automatically. A register address whose value doesn't change properly will be printed out in the code. (Here is the the full list of read-and-write register, on Confluence.)

Decision Making: See the next pages.

4.0.1 PowerUp Test - Decision Making

1. **DCRC Information**:
   Serial Number: Shows as labeled.
   MicroController Version: 2.09 (as of Feb 2020)
   Big FPGA Version: 21f5a28 (as of Sep 2020)
   Small FPGA Version: 0xb83a (as of Aug 2020)

2. **FPGA and microcontroller address/data Test:**
   GOOD: You get incremented values when reading Test Counter registers repeatedly. Message: ***OK***
   BAD: You don't get incremented values. Message:*"ERROR expected XXX but read YYY"*

3. **SDRAM Test:**
   GOOD: You read back the values you wrote. Message: **SDRAM Test OK***
   BAD: *"ERROR expected XXX but read YYY"*

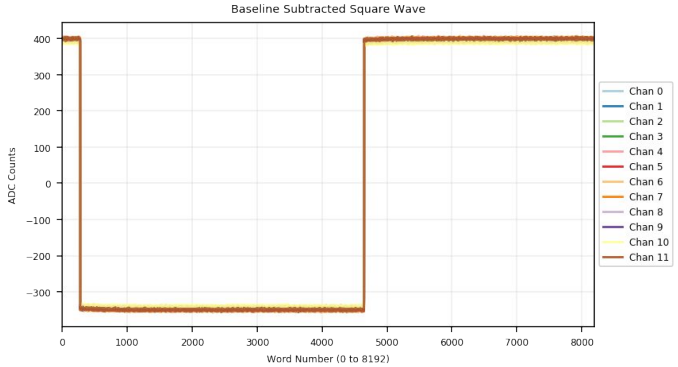
4. **ADC Readout Test:**
   GOOD: The two readout traces are identical. Message: ****ADC Readout Test Passed!****
   BAD: For each bad memory address the memory address, value of the first and second readout, and difference will be printed: *' Addr | Val1 | Val2 | Diff*

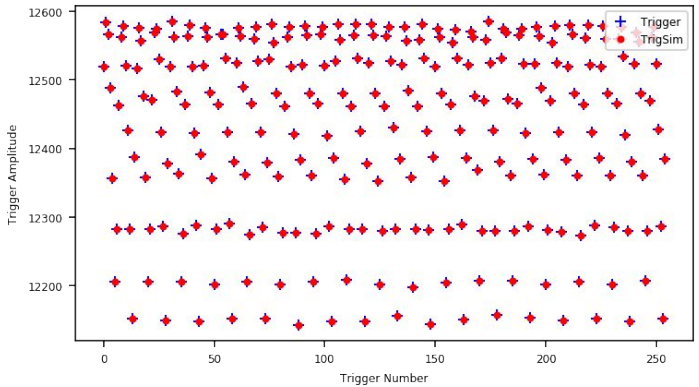
5. **Noise Traces Check**: See 4.1 Noise Test-traces & RMSs

4.0.1 PowerUp Test - Decision Making (contd)

6. **Phonon Trigger Test:** (see top plot)
   GOOD: 1) Square waves overlap and p2p amplitude vary no more than 50 adc counts*, indicating that we send the same square wave to each channel. 2) Message "GOOD! PhCh X is triggered. Amplitude matches trigger simulation" is printed, indicating the trigger get fired on each channel successfully. At the end "*PASS!! All PhChans are triggered*" message is printed, indicating all phonon channels are triggered.
   BAD: 1) Any part of the pulse trace shifts from the others or p2p difference is greater than 50 adc count. (See Appendix 0.0) 2) "*FAIL!! At least one PhChan is not triggered, or trigger amplitude doesn't match trigger simulation"* message is printed.

7. **Trigger and Trigger Simulation Amplitudes Comparison:** (See bottom plot)
   GOOD: 1) Trigger and trigger simulation amplitude are identical for all 255 trigger. *"***Trigger vs. Trigger Simulation Test is Passed!*** Discarding first XX points in trigsim"*
   BAD: Trigger and trigger simulation amplitudes are NOT identical.





* DrG: ×1. InG: ×0.99. PreAmp mode

4.0.1 PowerUp Test - Decision Making (contd)

8. **Phonon Inversion Test:** (See top plot)

GOOD: 1) Sine waves are plotted for ALL 12 phonon channels and all the traces overlap with each other and 2) peak to peak values vary by no more than 50 counts.

BAD: 1) Any trace inverted. Any part of any trace shifts from the others. (See Appendix 0.0) 2) Peak to peak values vary by more than 50 counts.

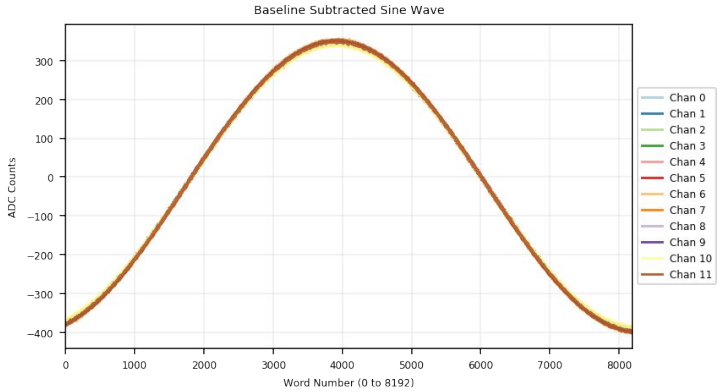
9. **Charge Offset:** See 4.3.0 Offset DAC Check

10. **Charge Pulse Injector Mapping:** (see bottom plot)

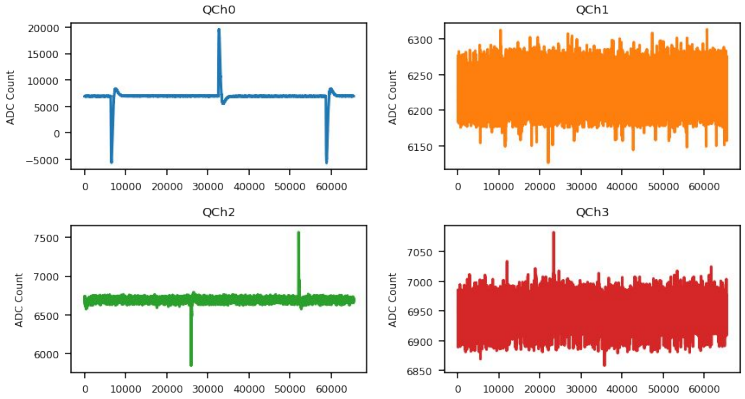
GOOD: The charge test pulser injector sends pulses to a specific channel, and we see the biggest pulse in that channel.

BAD: Pulses from Channel X show up in a different channel output.

11. **Charge Trigger Test**: See 4.3.1 Trigger Test w/ DCRC pulser



Sending pulses to QCh0, should see largest amplitude in QChan0.



4.0.1 PowerUp Test - Decision Making (contd)

12. **Random Trigger Test**

GOOD: 1) The random trigger is turned off, no random triggers recorded, and message "*PASS: Random trigger disabled and no random trigger recorded."* 2) The random trigger is turned on, random triggers recorded, and message "*PASS: Random trigger enabled and some random trigger recorded."*

BAD: The random trigger is turned off, random triggers recorded, and message *"FAIL: Random trigger disabled but some random trigger recorded!"* 2) The random trigger is turned on, random triggers are not recorded, and message "*FAIL: Random trigger enabled but no random trigger recorded!"*

13. **Readback Test:**

GOOD: "PASS!! All registers in Reg_Address1,2,3 are working properly." is printed below '4.4 Summary'.*

BAD: "FAIL!! Some registers do not work." is printed, as well as the list of busted registers.

* Four sections in the code, '4.1 Read-and-write registers', '4.2 Read-and-write bits','4.3 Registers that can control other registers', '4.4 Summary'. At the end of 4.1, 4.2 and 4.3, a 'PASS!! ... ' or 'FAIL!! ... ' message will be printed, which tells you if the registers pass the read back test or fail. At the end of '4.4 Summary', it will tell you the final result of Readback Test.

4. Tests and Calibration

4.0 Power-on test and PowerUp Test

4.1 Noise Tests (Traces&RMS, PSDs)

- 4.1.0 Traces&RMS check (Visually check traces are just noise and RMS is stable for each channel)
- 4.1.1 PSD check (Visually check PSDs meet the criteria)

4.2 Phonon Tests (Source Switch, InG&DrG, Trigger, Transfer Function)

4.3 Charge Tests (Offset DACs, Trigger)

4.4 Hybrid Readout Test

4.5 Calibration and DAQ Validating

4.1 Noise Tests - Overview

Goal: Plot the traces with no input (noise only) to check if they are typical. Convert to PSDs and check if they are good
Procedure: Read out 100 noise traces (no signal) from ADC for **ALL** channels, both phonon and charge channels, calculate the RMSs and use the 100 noise traces to calculate PSDs for each channel. Check traces, RMSs and PSDs for evidence of problems. Check if the PSDs pass the criteria. Repeat the same procedure for a complete set of tests*(phonon channels only, no PSD evaluation).

Decision Making:

Described in '**Visual (and Quantitative) Check**' in the next two pages.

Outputs:

1. Data Plots: Traces and PSDs for ALL phonon channels with various gain settings and ALL charge channels
2. Test Result Summaries: features different from typical results, pass/fail the test. Will be posted on Confluence (RevE. Prod.).

* a complete set of tests(Noah's proposal and notes):

1. Pre/Post DrG noise: InG fixed at ×0, DrG(×2, ×8); both in preamp/open loop
2. Pre/Post InG noise: DrG fixed at ×8, InG(×-1, ×-2, ×2); all in preamp/open loop
3. Closed-loop noise: DrG fixed at ×8, InG(×-1, ×-2, ×-4); both in feedback/closed loop
4. Small DrG noise: DrG fixed at ×1, InG(×-1, ×-2), preamp/open loop

From these we can pretty much determine what's on the board and what's in the environment. It may not be super helpful from a pure board functionality standpoint, but it will probably be helpful in sensing whether there's some flaw in the board allowing extra noise.

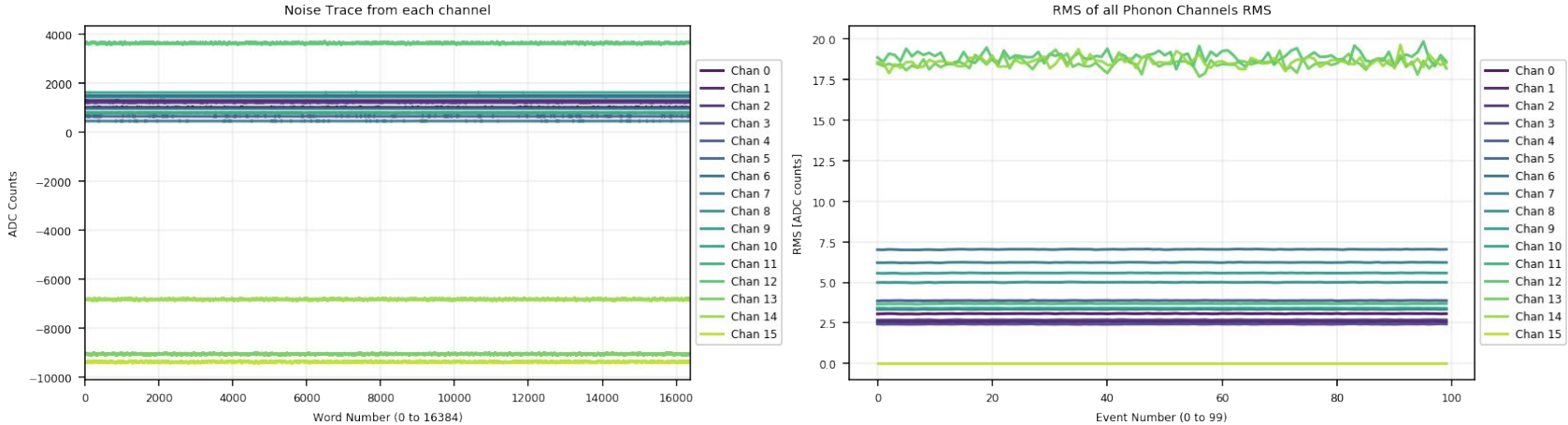
4.1 Noise Test - Traces and RMSs

The LHS plot shows the traces for single readout events, and the RHS plot shows the RMSs of each trace from 100 different readout events. (SN21, DrG(×1) and InG(+0), Preamp/Open loop, tested in Sep, 2019) (Click here, RevE and Prod, for more results)

Visual Check

GOOD: ALL traces in the LHS plot are flat (with fluctuation) as function of time. RMS 'traces' in the RHS plot are all flat, variation seeming to be random around the mean.

BAD: 1) In the LHS plot, any trace is at the maximum(+32678) or minimum value(-32678), shown in Appendix 1.1. If changing the charge offset doesn't change the ADC value, it's bad. 2) For the trace in LHS plot, there is any spike/peak. Test one more time. If it happens again, it shouldn't be caused by electrical transient and we will report it. For each RMS 'trace' in the RHS plot, there is any RMS value 50% higher than the others on the same 'trace'. (See bad results in Appendix 1.1.)



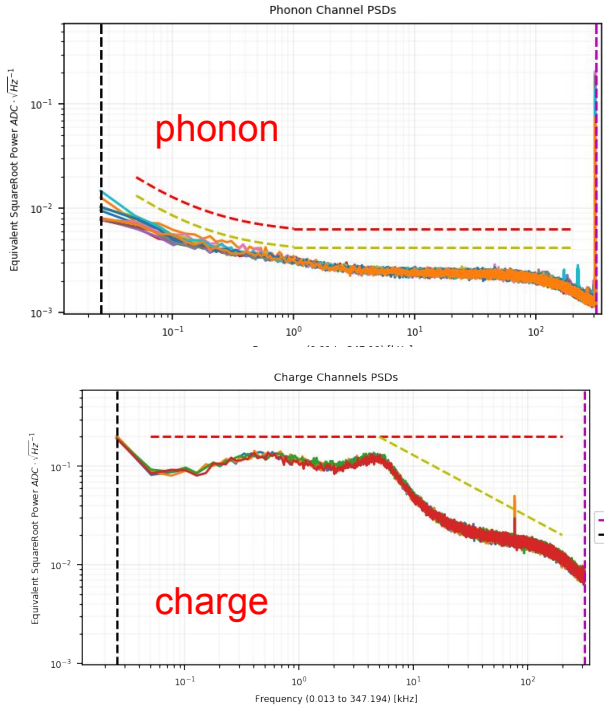
4.1 Noise Test - PSD Evaluation

(See more phonon PSDs in Appendix 1.2 Typical Phonon PSDs, w/o evaluation)
(Check the full sets results here, RevE and Prod.)

Visual and Quantitative* Check (50Hz-200kHz)**:
Phonon PSDs:
GOOD: All 12 PSDs overlap each other, 50Hz-200kHz are below the yellow dashed line. **Warning**: For each PSD, 1 to 3 frequencies higher than the yellow dashed line but lower than the red dashed line. It's not a failure, but better to be noticed.
BAD: 1) Any frequency hits the red dashed line. 2) More than 3 frequencies higher than the yellow dashed line. 3) Any channel's PSD shifted from others. See examples in Appendix 1.2 examples of bad PSDs.
Charge PSDs:
GOOD: All 4 PSDs overlap each other, 50Hz-200kHz are below the yellow dashed line. **Warning**: 1 to 3 frequencies higher than the yellow dashed line but lower than the red dashed line. It's not a failure, but better to be noticed.
BAD: 1) Any frequency hits the red dashed line. 2) More than 3 frequencies higher than the yellow dashed line. 3) Any channel's PSD shifted from others. See examples in Appendix 1.2 examples of bad PSDs.

Note: If there is any feature visually different, e.g. peaks/bumps/spikes, from typical results, notes will be made on Confluence(RevE Prod).

SN63, Preamp/Open loop, DrG(×1), InG(×0.99) , Aug 2020



* We have set the standard for evaluating phonon PSD and are automating it in the code. See here for more technical info.
** There is no need to check the PSD higher than 200kHz. Click here for more technical info.

4. Tests and Calibration

4.0 Power-on test and PowerUp Test

4.1 Noise Tests (traces, RMS, PSDs)

4.2 Phonon Tests (Source Switch, InG&DrG, Trigger, Transfer Function)

- 4.2.0 Source Switch Check (Visually check switches in all phonon channels work)
- 4.2.1 InG & DrG Check (Amplitudes of the test signal will change correctly as the InG and/or DrG change)
- 4.2.2 Trigger Check (Check triggers all work by seeing triggered pulses)
- 4.2.3 Transfer Function Measurement (Measure transfer function for all phonon channel, amplitude only)

4.3 Charge Tests (Offset DACs, Trigger)

4.4 Hybrid Readout Test

4.5 Calibration and DAQ Validating

4.2 Phonon Test - Overview

Goal: Check Source Switch and Trigger work. Check InG, DrG and feedback loop work as designed.
Procedure: (**Source Switch**)Set the internal signal generator to send a sine wave signal to DCRC, plot the traces read out from DCRC ADC in preamp mode and feedback mode and visually check the traces. (**InG & DrG**) Set the internal signal generator to send a sine wave signal to DCRC, read out the traces from DCRC ADC, measure the amplitudes and quantitatively check if the amplitude varies with gain properly. (**Trigger**) Set the picoscope to send a pulse to DCRC via SMB port and read out trace from DCRC ADC in preamp mode and feedback mode. Traces will be plotted if the trigger gets fired. (**Transfer Function**) Set the picoscope to send sine wave signals with various frequencies. Read out the trace from DCRC ADC, calculate the amplitudes and make 'amplitude vs frequency' plots for all phonon channels.

Decision Making:

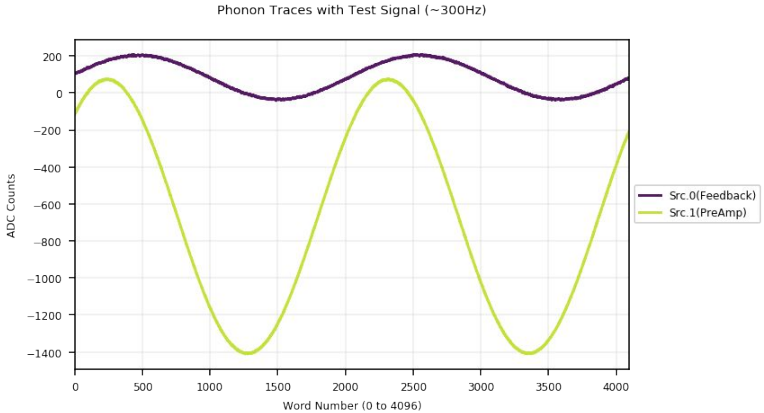
1. **Source Switch**: It's good if you see sine waves in both preamp and feedback modes. Visual check only
2. **InG & DrG**: Visual check and quantitative check.
    - 2.1. Check **InG**: With DrG fixed, check the amplitude varies linearly with InG in preamp/open mode and inversely linearly in feedback/closed mode.
    - 2.2. Check **DrG**: With InG fixed, check the amplitude varies linearly with DrG. Tested in preamp/open mode
3. **Trigger**: It's good if the triggered pulse and FIR output are plotted, which indicates the trigger get fired and the amplitude is higher the threshold and matches the trigger simulation. It's bad if "Channel X is not triggered" and a mismatch message printed out during the test and. Visual Check Only.
    - 3.1. Trigger test will be done in preAmp/open mode and feedback/closed mode separately

Typical results: (See next slides)

4.2.0 Phonon Test - Source Switch

Goal: Check Source Switches in all 12 phonon channels work.
Procedure: We set the internal signal generator to send a sine wave signal to DCRC in both Preamp/open mode and Feedback/closed mode. Traces read out from DCRC ADC will be plotted for all phonon channels. The offsets and amplitudes will be calculated and displayed as well(No check required). (Setting: DrG: 0(×1). InG: 0xea(-0.99))

Visual Check:
GOOD: 1. Two sine waves are displayed in the plot(like the LHS plot) for ALL 12 phonon channels. The one from feedback mode is with smaller amplitude and the other from preamp mode is with larger amplitude. (Marked with red squares)
BAD : 1. No sine wave, indicating somewhere is broken; 2. Two sine waves have the same amplitude, indicating the switch gets stuck at one position.



	Src.0(Feedback)		Src.1(PreAmp)	
	offset0	Amp0	offset1	Amp1
Chan.0	426.5	121.5	1122.0	750.0
Chan.1	-619.5	122.5	645.5	745.5
Chan.2	409.5	121.5	1347.5	742.5
Chan.3	1.5	123.5	618.0	734.0
Chan.4	-522.0	124.0	297.0	741.0
Chan.5	-676.0	119.0	298.0	757.0
Chan.6	-1554.5	121.5	-701.5	741.5
Chan.7	-294.0	122.0	315.0	737.0
Chan.8	222.0	121.0	1043.0	750.0
Chan.9	-710.0	124.0	575.5	726.5
Chan.10	457.0	121.0	1262.5	737.5
Chan.11	314.5	122.5	798.5	734.5

4.2.1 Phonon Test - InG & DrG

Goal: Check the InGs and DrGs work as designed.
Procedure: Set the internal signal generator to send sine wave signals to DCRC, read out the traces from DCRC ADC, measure the amplitudes and quantitatively check if the amplitude varies with gain properly. 1) The amplitude vary **linearly** with DrG*. 2) The amplitude vary **linearly** with InG in preamp mode and **inversely linearly** with InG in feedback mode***.
Settings:

1. Check DrG: InG fixed (at ×4.01), DrG(×1, ×2, ×4, ×8), preamp/open mode;
2. Check Positive InG: DrG fixed (at ×4), InG(×0.99, ×1.98, ×2.97, ×4.01, ×5.00, ×5.99), preamp mode;
3. Check Negative InG: DrG fixed (at ×4), InG(×-0.99, ×-1.98, ×-2.97, ×-4.01, ×-5.00, ×-5.99), feedback mode

Visual Check:
GOOD: Amplitude varies as expected when InG and DrG change, see more in next three slides.
BAD : The amplitude doesn't change properly.

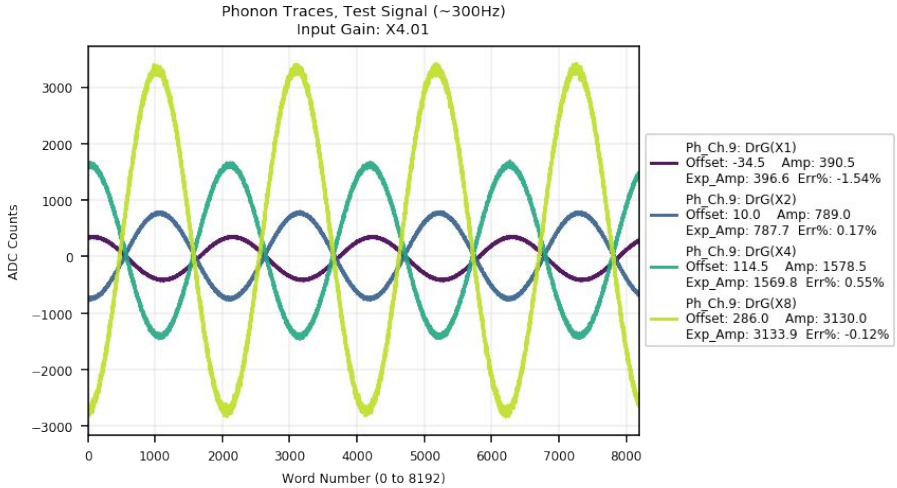
Quantitative Check:
GOOD: The relative errors(Err%)** of amplitudes are good. See more in the next three slides.
BAD: Some values of relative errors are large.

* DrG test is done in preamp mode. It is not necessary to do both according to the RevE Phonon Block design.
** Err% = (Amp - Exp_Amp/Exp_Amp. Amp is the measured value in adc channel. Exp_Amp is the expected value which is calculated by linearly fitting the measured valued. If the linearity if not good enough, the Err% will be large.
*** Technical attachment.

4.2.1 Phonon Test - DrG

Goal: Check amplitude varies **linearly** with DrG.
Procedure: Described in the previous slide.
Settings: InG fixed (at ×4.01), DrG(×1, ×2, ×4, ×8), preamp/open mode

Visual Check:
GOOD: Amplitude varies as DrG changes.
BAD : The amplitude doesn't change as DrG changes.
Quantitative Check:
GOOD: ALL Err% in the legend are < 2%*, which indicates amplitude varies **linearly** and the **linearity** is good.
BAD : Some values are larger than 2%.



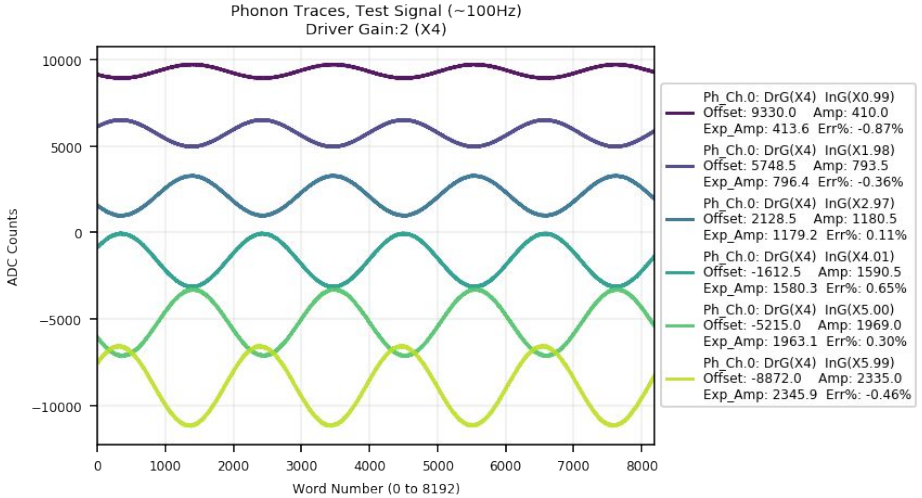
(results of SN30, tested on July, 2020)

* 2% is set based on the Err% values of a working board. We use it as the standard until people request or tell us a more restrictive tolerance. In fact, most Err% values are <1%, but it's not a requirement.

4.2.1 Phonon Test - InG (positive)

Goal: Amplitude varies **linearly** with InG in preamp/open mode
Procedure: Described in a previous slide.
Settings: DrG fixed (at ×4), InG(×0.99, ×1.98, ×2.97, ×4.01, ×5.00, ×5.99), preamp/open mode

Visual Check:
GOOD: Amplitude varies as InG changes
BAD : The amplitude doesn't change as InG changes.
Quantitative Check:
GOOD: ALL Err% in the legend are <2%*, which indicates amplitude varies linearly and the linearity is good
BAD : Some values are larger than 2%.



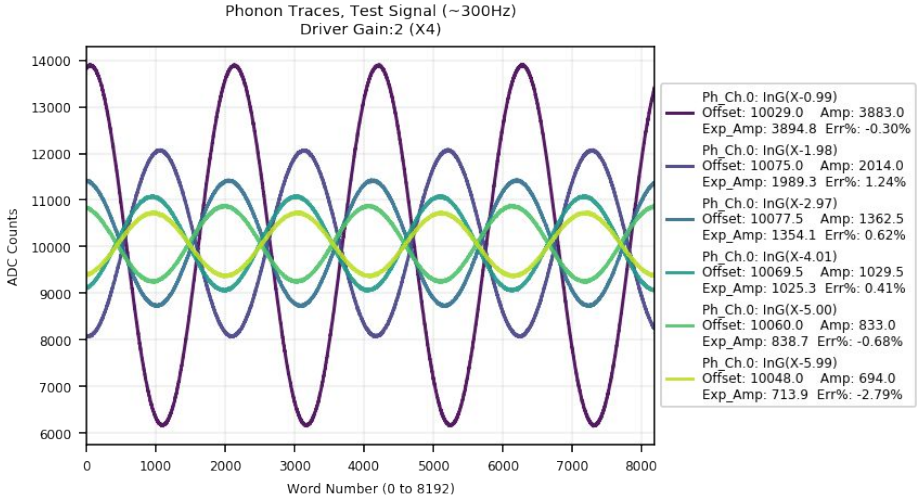
(results of SN21, tested on Jan 20, 2020)

* 2% is set based on the Err% values of a working board. We use it as the standard until people request or tell us a more restrictive tolerance. In fact, most Err% values are <1%, but it's not a requirement.

4.2.1 Phonon Test - InG (negative)

Goal: Amplitude varies **inversely linearly** in feedback/closed mode.
Procedure: Described in a previous slide.
Settings: DrG fixed (at ×4), InG(×-0.99, ×-1.98, ×-2.97, ×-4.01, ×-5.00, ×-5.99), feedback/close mode

Visual Check:
GOOD: Amplitude varies as InG(negative) changes
BAD : The amplitude doesn't change as InG(negative) changes.
Quantitative Check:
GOOD: ALL Err% in the legend are <3%, which indicates amplitude varies inversely linearly as InG(negative) changes and the inverse linearnarity is good.
BAD : Some values are much larger than 3%.



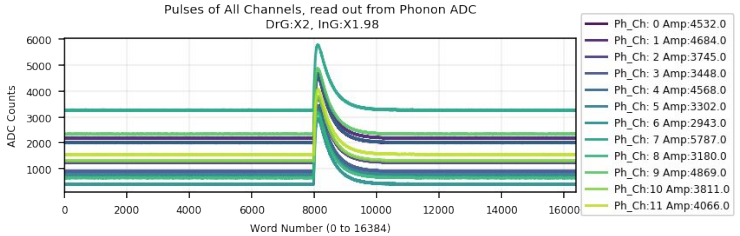
(results of SN21, tested on Jan 20, 2020)

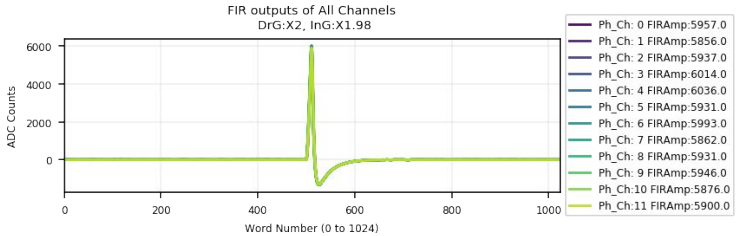
* 3% is set based on the Err% values of a working board. We use it as the standard until people request or tell us a more restrictive tolerance. In fact, most Err% values are <2%, but it's not a requirement.

4.2.2 Phonon Test - Trigger Test

Goal: Check that the trigger gets fired successfully and works as designed.
Procedure: Set the picoscope to send a pulse that approximates the shape of a phonon pulse to phonon channels via SMB port individually. The trigger will get fired if the FIR amplitude is higher than the threshold, then the trace of pulse will be read out from DCRC ADC. In addition, we send the pulse data to the trigger simulation and read out the FIR output. By comparing the amplitudes of FIR output against the one from trigger simulation, we can check if the trigger works as expected and trigger simulation works in accordance with real trigger pulses. Pulses and FIR outputs will be plotted if everything is good.

Visual Check: (plots with preamp mode shown)
GOOD: **ALL** 12 triggered pulses, upward in preamp mode and downward in feedback mode, are displayed in the plot.
BAD: Any pulse is missed and “Ch.X is not triggered” is printed, which indicates it fails to record any triggered pulse. (maybe the threshold is set too high)



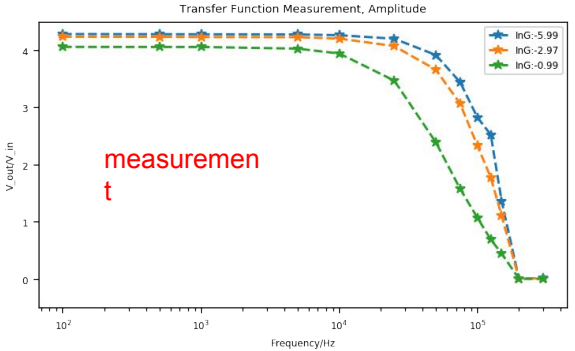


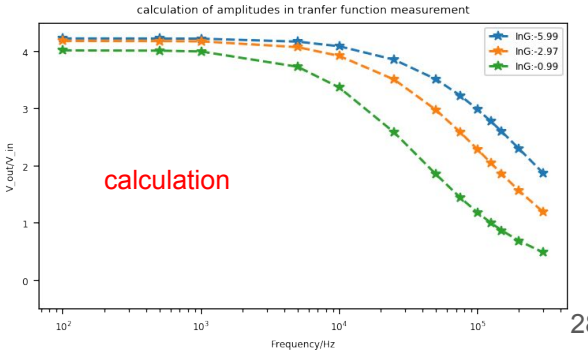
Quantitative Check (will be done automatically by code):
GOOD: 1. The FIR amplitude is higher than the threshold; 2. The trigger amplitude matches the trigger simulation.
BAD: 1. Fail to trigger, “tried 10 times, but recorded no triggers” printed; 2. A message printed indicating the trigger amplitude does not match trigger simulation.

4.2.3 Transfer Function Measurement

Goal: Check the feedback loop works as expected.
Procedure: Send sine waves with various frequencies through SMB port, read out the traces from Phonon ADC, calculate the amplitudes and make 'V_out/V_in* vs frequency' plots for all phonon channels. Repeat the procedure for all channels.
Setting: Frequency, 100Hz-300kHz; InG, -5.99, -2.97, -0.99, Mode: Feedback mode

Visual and Quantitative Check:
(top plot: measured ratio; bottom plot: calculated ratio**)
GOOD: 1) The measured ratios are 4.0-4.5 at low frequency (100Hz-10kHz), start to drop at 10kHz, and drop to almost zero at 200kHz. 2) The measured ratios are consistent with the calculation at low frequency (100-1000Hz)**. 3) blue curve > yellow curve > green curve.
BAD: 1) the ratios are <4.0 or >4.5 at low frequency (100Hz-10kHz). 2) The order of the three curves does not match the calculation(blue curve > yellow curve > green curve).





* V_out is the amplitude calculated from the trace and V_in is amplitude of the sine wave signal at SMB port
** See the deduction in *DCRC math.ipynb*. The calculation considers only the capacitor's frequency dependence, so it's not surprise the deviation at high frequency.

4. Tests and Calibration

4.0 Power-on test and PowerUp Test

4.1 Noise Tests (traces, RMS, PSDs)

4.2 Phonon Tests (Source Switch, InG&DrG, Trigger, Transfer Function)

4.3 Charge Tests (Offset DACs, Trigger)

- 4.3.0 Offset DAC Check (Visually check traces after changing the charge offsets)
- 4.3.1 Trigger Test (Check all triggers work by seeing triggered pulses)

4.4 Hybrid Readout Test

4.5 Calibration and DAQ Validating

4.3 Charge Test - Overview

Goal: Check that the four charge offset DACs were built correctly and consistently and that trigger works.
Procedure: (**Offset DAC Check**) We change the charge offset for all four charge channels and plot the traces read out from DCRC ADC to see if they change as expected.
(**Trigger Test**) We set the picoscope to send a simulated charge pulse to each channel via SMB port individually. If the trigger gets fired successfully, the pulse will be read out from DCRC ADC and plotted as well as FIR output.

Decision making process:

1. **Offset DAC Check**: 1)For each charge channel, one curve's endpoint should be at the same level as the starting point of another. 2) The relative change between levels and the rise/fall times are roughly same among the four charge channels. (visual check only)
2. **Trigger Test**: Two signal sources will be used, the charge pulser and external signal generator (picoscope). All triggers should get fired successfully with both signal sources and the trigger amplitudes match the trigger simulation.

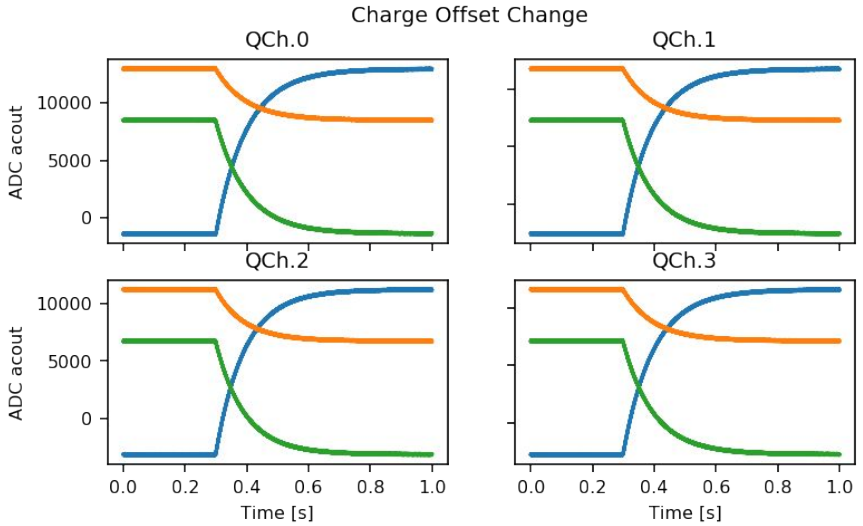
Typical results:

(See next slides)

4.3.0 Charge Test - Offset DAC Check

Goal: Check that the charge offset DACs of all four charge channels were built correctly and consistently.
Procedure: We change the charge offset to three values (marked **blue**, **orange**, **green**) in turn, read the traces out from DCRC ADC individually and plot them to see if they are good/typical. As the charge offset is changed, the trace will rise/fall to the level we set. (Rise/Fall times are not measured in this test.)

Visual Check Only:
GOOD: 1. In each plot, the endpoint of the **blue** curve is at the same level as the starting point of the **orange** curve, and that the end point of the **orange** curve is at the same level as the starting point of the **green** curve. 2. The levels of the three curves(**blue**, **orange**, **green**) in these four plots don't have to be exactly the same, but the relative change should be the same. 3. The rise/fall time are roughly the same..
BAD: If the relative change between levels or the rise/fall times for one channel were much different from the other channels, that would tell us that (probably) something in the charge offset DACs (including the amplifiers and low-pass filters) was messed up -- perhaps an open circuit or short circuit, or the wrong value resistor or capacitor somewhere.

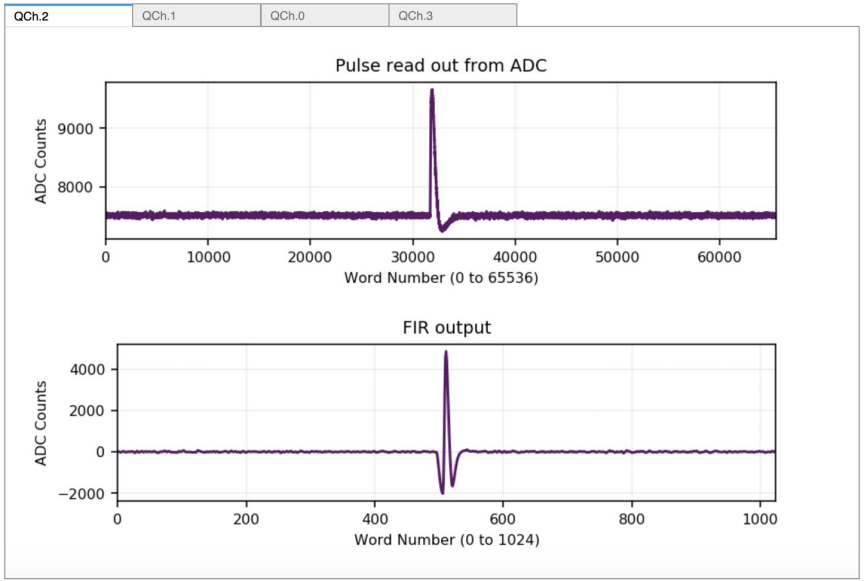


4.3.1 Charge Test - Trigger Test w/ DCRC pulser

Goal: Check the charge pulse injector works, and the trigger gets fired successfully and works as designed.
Procedure: We enable the charge pulse test and send the pulse to each charge channel. The trigger will get fired if the FIR amplitude is higher than the threshold, then the trace of pulse will be read out from DCRC ADC. In addition, we send the pulse data to the trigger simulation and read out the FIR output. By comparing the amplitudes of FIR output against the one from trigger simulation, we can check if the trigger works as expected and trigger simulation works in accordance with real trigger. pulses will be plotted if everything is good.

Visual Check: (Top, pulse from ADC; Bottom, FIR output)
GOOD: Pulses are displayed (**must be upright**) for ALL four charge channels.
BAD : 1. Any pulse is missed and “Ch.X is not triggered” is printed, which indicates it fails to record any triggered pulse. (maybe the threshold is set too low) 2. The pulse that goes downward indicates some issue with the charge channel or the trigger setting.

Quantitative Check (will done automatically by code):
GOOD: 1. The FIR amplitude is higher than the threshold; 2. The trigger amplitude matches trigger simulation.
BAD: 1. Fail to trigger, “tried 10 times, but recorded no triggers” printed; 2. A message printed indicating the trigger amplitude does not match the trigger simulation.

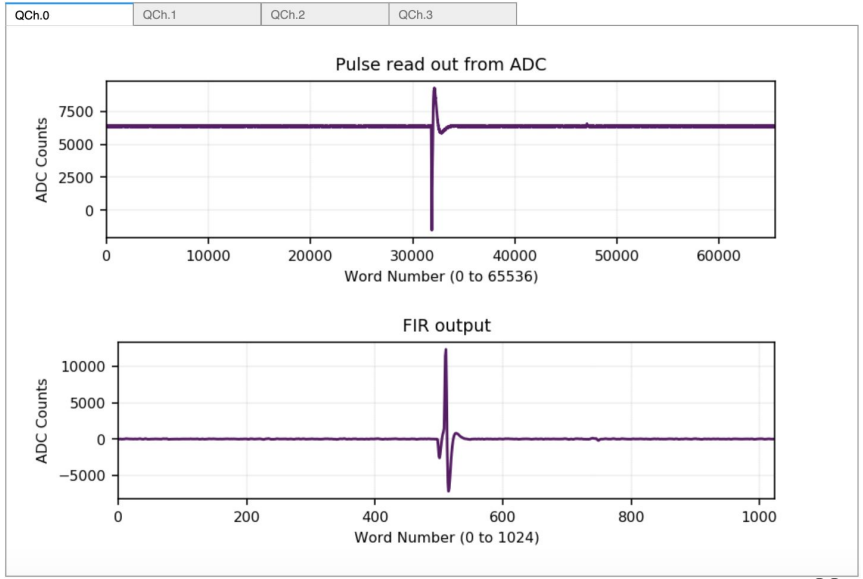


4.3.1 Charge Test - Trigger Test w/ external pulse

Goal: Check the trigger gets fired successfully and works as designed.
Procedure: We set the picoscope to send a pulse that approximates the shape of a charge pulse and send it to each charge channel via SMB port individually. The trigger will fire if the FIR amplitude is higher than the threshold, then the trace of pulse will be read out from DCRC ADC. In addition, we send the pulse data to the trigger simulation and read out the FIR output. By comparing the amplitudes of FIR output against the one from trigger simulation, we can check if the trigger works as expected and trigger simulation works in accordance with real trigger. Pulses will be plotted if everything is good.

Visual Check: (Top, pulse from ADC; Bottom, FIR output)
GOOD: Pulses are displayed for ALL four charge channels.
BAD : Any pulse is missed and "Ch.X is not triggered" is printed, which indicates it fails to record any triggered pulse. (maybe the threshold is set too high)

Quantitative Check (done automatically by code):
GOOD: 1. The FIR amplitude is higher than the threshold; 2. The trigger amplitude matches trigger simulation.
BAD: 1. Fail to trigger, "tried 10 times, but recorded no triggers" printed; 2. A message printed, indicating the trigger amplitude does not match trigger simulation.



4. Tests and Calibration

4.0 Power-on test and PowerUp Test

4.1 Noise Tests (traces, RMS, PSDs)

4.2 Phonon Tests (Source Switch, InG&DrG, Trigger, Transfer Function)

4.3 Charge Tests (Offset DACs, Trigger)

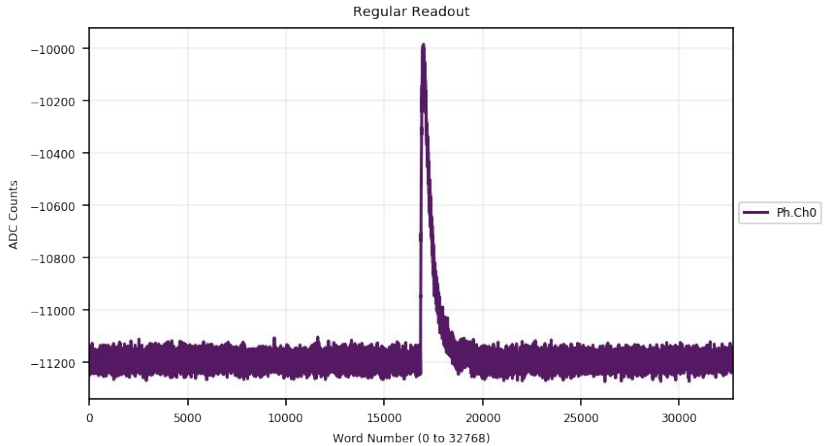
4.4 Hybrid Readout Test

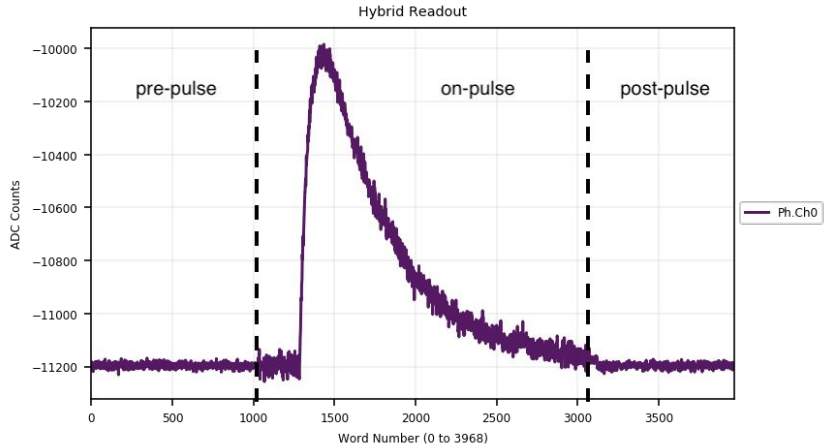
4.5 Calibration and DAQ Validating

4.4 Hybrid Readout Test

Goal: Check Hybrid readout work as expected.
Procedure: Read out a chunk of data without downsampling, as the left plot shows. Set up the downsampling and read out the same chunk of data with part of it downsampled (i.e. hybrid readout, 16 bins combined as one for pre-pulse and pose-pulse), as the right plot shows. Compare what you get against a calculation of what it should be from the full-rate data, which is done by the code automatically. (Hybrid readout focuses on the pulse itself and records less non-pulse data.)

Visual Check:
GOOD: The pulse was read out with full rate (on-pulse), and the pre-pulse and post-pulse are less noisy than the pulse.
BAD: 1)The on-pulse region was read out with downsampling.





4.4 Hybrid Readout Test (continued)

Quantitative Check:

GOOD: All results are **True**, indicating data in hybrid readout are equal to the calculation of what it should be from the full-rate data

BAD: There is any **False**. Investigate why.

```
1 all((fullrate[:16*prepulse].reshape(prepulse,16).sum(axis=1) >> 4) == hybrid[:prepulse])
```

```
True
```

```
1 all(fullrate[16*prepulse:16*prepulse + onpulse] == hybrid[prepulse:prepulse+onpulse])
```

```
True
```

```
1 all((fullrate[16*prepulse+onpulse:].reshape(postpulse,16).sum(axis=1) >> 4) == hybrid[prepulse+onpulse:])
```

```
True
```

4. Tests and Calibration

4.0 Power-on test and Pre-Test

4.1 Noise Tests (traces, RMS, PSDs)

4.2 Phonon Tests (Source Switch, InG&DrG, Trigger, Transfer Function)

4.3 Charge Tests (Offset DACs, Trigger)

4.4 Hybrid Readout Test

4.5 Calibration and DAQ Validating

4.5 Calibration -- Overview

Procedure and Goal:
Set the register values and measure the voltages on the corresponding pins. Initially we use the designed slopes and default offset of 0.0 to estimate the voltages. The calibration code will tell picoscope to use the best offset and range(with the minimum error) to measure the voltage. Then we use the measured values to calculate the slopes and offsets as well as their uncertainties for all registers. This will check that the calibration registers work and the real functions of voltages to register values. During the procedure, make sure every measurement is good, then fill in those numbers into the spreadsheet(template) and produce the MIDAS file at the end.

- slope: xx mV/step | offset: xx mV, and their uncertainties.

Decision Making and Typical Results:

- See the next two slides

Output: MIDAS file with calibration constants for each board.

- file name format: revE0_XX.cal
- will be committed to the online/src/DCRC/calibrations/ directory of the MidasDAQ repository (http://titus.stanford.edu:8080/git/tree/?f=online/src/DCRC/calibrations&r=DAQ/MidasDAQ)

Appendix: more details about the calibration procedure.

4.5 Calibration - Decision Making

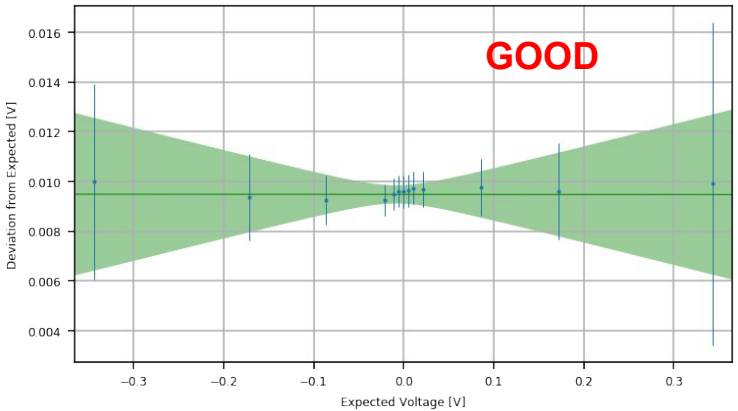
Make sure every measurement is good by visual check. Fill in the slopes and offsets into the spreadsheet if the measurement is good.

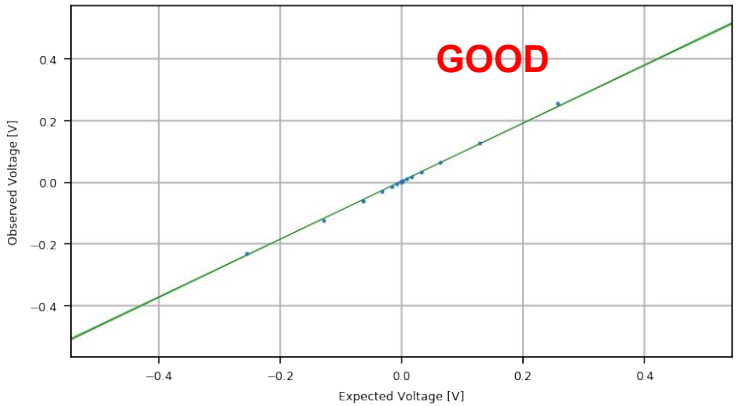
Visual Check:

- Designed Voltage = Designed Slope × Register Value
- Observed Voltage = Observed Slope × Register Value + Observed Offset

GOOD: In LHS plot, ALL the points are inside the green shadow region. In RHS plot, ALL the points are along the green line (fitting), no point far away. Both combined indicate the measurement is good and the measured values are reliable.

BAD: In LHS plot, any point outside the green shadow retion. In RHS plot, any point is far away from the green line. See bad example in Appendix 2.1. Either of them indicates the measurement is bad. Maybe the picoscope probe lost contact with the pin during measurement.





4.5 Calibration - Typical Results

Quantitative Check (Done automatically in the code):

GOOD: The slope and offset values are within tolerance. The values will be recorded.

BAD: The slope and offset values are beyond tolerance.

Category	Designed Slope Value on J-pin/Resistor	Measured Value +- Measurement Error (a typical result, S: Slope, O: Offset)	Tolerance* (S: Slope, O: Offset)
DDSMagnitude	**1.857 mV/step**	**S: 1.882±0.010 mV/step O: 0.11±0.93mV**	**S: 1.887±0.015 mV/step O: 0.095±0.085 mV**
Driver Offset	**0.125 mV/step**	**S: 0.1256±0.0012 mV/step O: 12.6±0.4 mV**	**S: 0.1251±0.0011 mV/step O: 13±43 mV**
LockPoint	**0.125 mV/step**	**S: 0.1251±0.0012 mV/step O: 0.5±0.3 mV**	**S: 0.1252±0.0012 mV/step O: 12±38 mV**
SqdBias	**0.125 mV/step**	**S: 0.1255±0.0012 mV/step O: 20.1±0.4 mV**	**S: 0.1250±0.0012 mV/step O: 10±37 mV**
QETBias	**0.0839 mV/step**	**S: 0.0829±0.0008 mV/step O: 11.0±0.4 mV**	**S: 0.0835±0.0012 mV/step O: 9±25 mV**
QOffset	**0.125 mV/step**	**S: 0.1248±0.0012 mV/step O: -3.7±0.3 mV**	**S: 0.1248±0.0010 mV/step O: 0±46 mV**
QBias	**0.42725 mV/step**	**S: 0.3935±0.0038 mV/step O: 79.2± 0.8 mV**	**S: 0.3924±0.0021 mV/step O: 94±91 mV**
LEDMagnitude	**0.2442 mV/step**	**S: 0.2454±0.0025 mV/step O: -1.0±0.6 mV**	**S: 0.2449±0.0037 mV/step O: -1±8 mV**

* The tolerance for each category was set by collecting the measured values from SN30, SN31 and SN63 and calculating the range, **mean+-3*RMS**.

4.5 Calibration - Validating with DAQ

Goal: Check DCRC with MIDAS DAQ will be operated in the same way as at SNOLAB and test facilities.
Procedure: We spot check by randomly setting 3 channels of *ADCOffset*, *LockPoint*, *SQUIDBias*, *AmpOffset* to zero and physically measure them on the DCRC with picoscope(ZeroPoint Check). We check *QETBias* on minibob and *Test Signal* amplitude for multiple ODB values, measure voltages on the DCRC and calculate the slope and offset (SlopeOffset Check).

Visual and Quantitative Check:
GOOD: 1. For *ADCOffset*, *LockPoint*, *SQUIDBias*, *AmpOffset*, the measured voltages are within ranges (see LHS table) after setting the value to zero on DAQ. 2. For *Test Signal*, *QETBias*, *LED Current,* their validation slopes and offsets are within the ranges(See RHS table).
BAD: 1. *ADCOffset*, *LockPoint*, *SQUIDBias*, *AmpOffset*, voltages are out of the tolerance range. *QETBias* and *TestSignal* plots aren't linear.

	Check Type	Tolerance
ADCOffset	ZeroPoint	(-1.5 mV, +1.5 mV)
LockPoint	ZeroPoint	(-1.5 mV, +1.5 mV)
SQUIDBias	ZeroPoint	(-1.5 mV, +1.5 mV)
AmpOffset	ZeroPoint	(-1.5 mV, +1.5 mV)
QBias	ZeroPoint	(-1.5 mV, +1.5 mV)

	Check Type	Tolerance
Test Signal	SlopeOffset	Slope, 1.000±0.015; Offset, 0.0±0.5 mV
QETBias	SlopeOffset	Slope, 1.000±0.015; Offset: 0±3.5 μA (0±3.5 mV, J-pin/miniBob)
LED Current	SlopeOffset	Slope, 1.000±0.015; Offset: 0±20 μA (0±2 mV, R699)

4.5 Note on Connector Testing

We have a number of connectors on the board. We do not need a specific set of connector tests because each is tested in process of doing the other tests. For completeness we note all the connectors and list at least one test for each that would have failed if the connector were broken:

- Ethernet
- SMBs on miniBOB

5. Proposal

- We propose that the procedures described in this talk be used to verify and calibrate all DCRC RevE/Prod boards before sending to SNOLAB
- Unless there are objections we will proceed as planned.

Testing not included in this version

- **New LED test**: A new feature of LED current/voltage waveforms readout will be added. FNAL is still working on the 1st stage, modifying a board to test. The related test will be a second pass.
- **Thermometry Test**. Seems SLAC will take care of it.

6. Conclusion

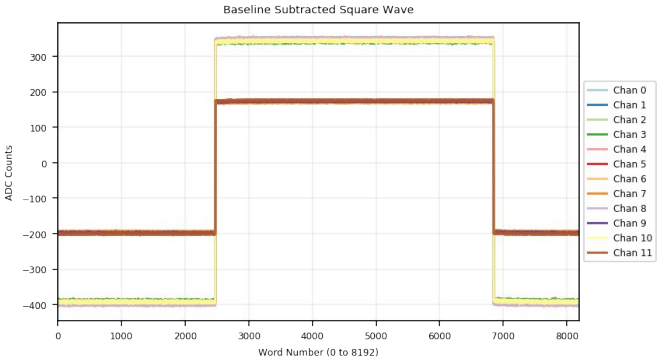
We have developed a large set of procedures and accompanying documentation for testing and calibrating the DCRC RevE/Prod boards.

The procedures have caught many problems, and the boards which have been sent to other facilities have worked well (modulo updating our procedures)

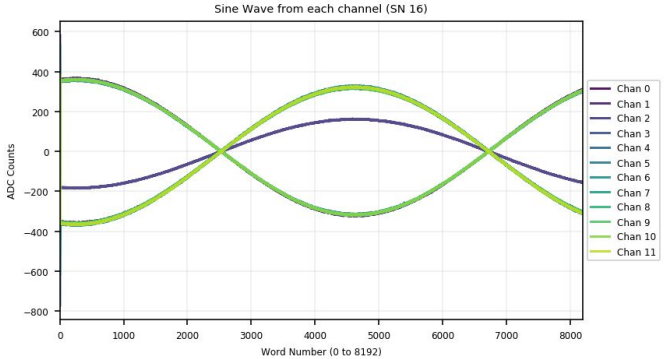
We propose this testing and calibration procedure as the official procedure for use in testing and calibrating the DCRC RevE/Prod Boards.

7. Appendix 0.0, BAD results of PowerUp Test

Here is an example plot of bad result of trigger test in PowerUp Test.
- Square waves have different amplitudes

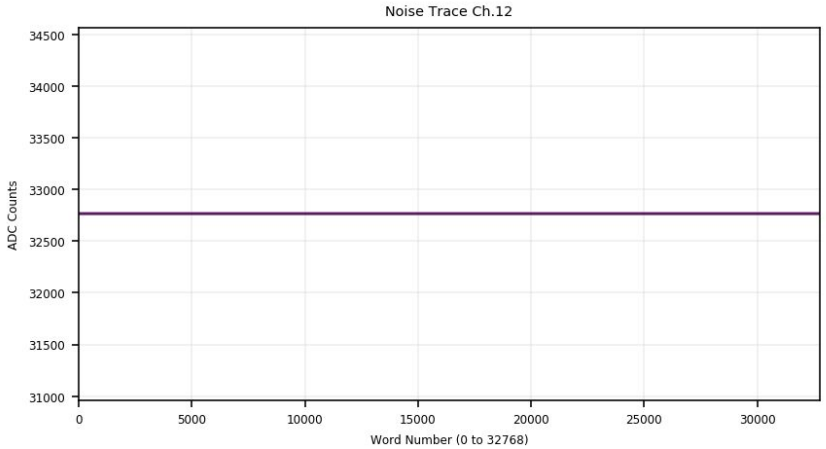


Here is an example plot of bad result of inversion check in PowerUp Test.
- We see some inverted channels and different amplitudes

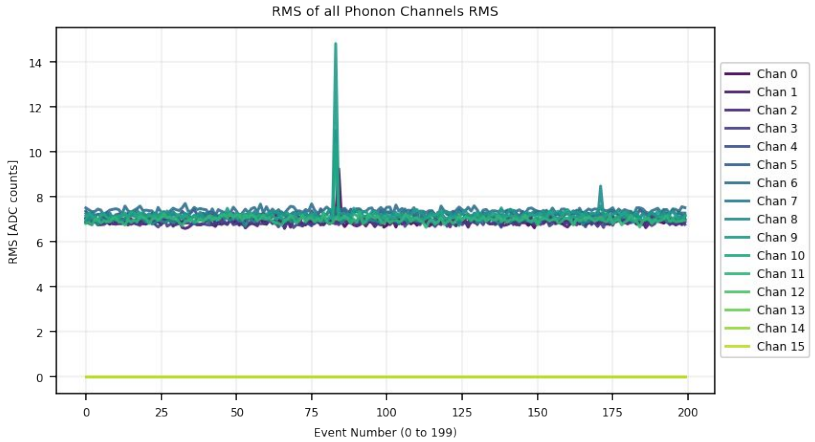


7. Appendix 1.1, Bad Noise Trace and Bad ‘RMS’ Trace

If the offset was set too large, out of the range (-32768, 32768), the trace would become just a flat line at the max or at the min. The below the example of upper railed trace, a flat line at 32768.

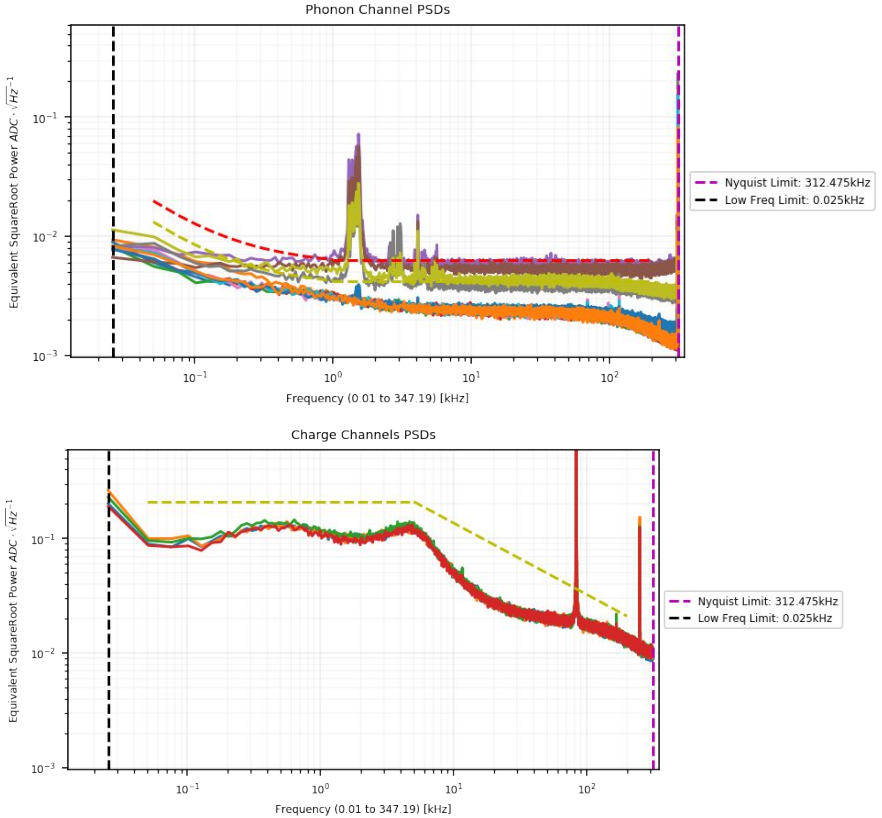


There will be some RMS values higher the others, which might be caused by electronic devices beside the DCRC board.



7. Appendix 1.2, examples of BAD PSDs

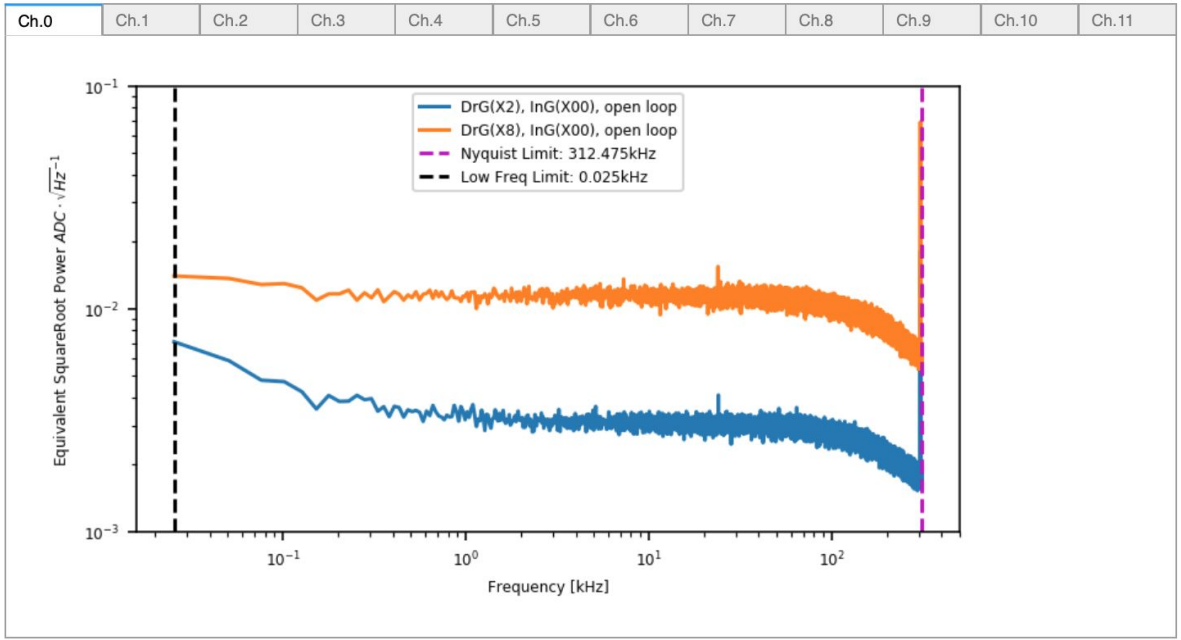
Top: BAD phonon channel PSDs
Bottom: BAD charge channel PSDs



7. Appendix 1.2, Typical Phonon PSDs, Pre/Post DrG.

Board: SN49, tested on Sep 3, 20120.
Setting:

Src: PreAmp/Open Mode.
InG: 0x00(X0.00).
DrG: 1(X2); 3(X8).

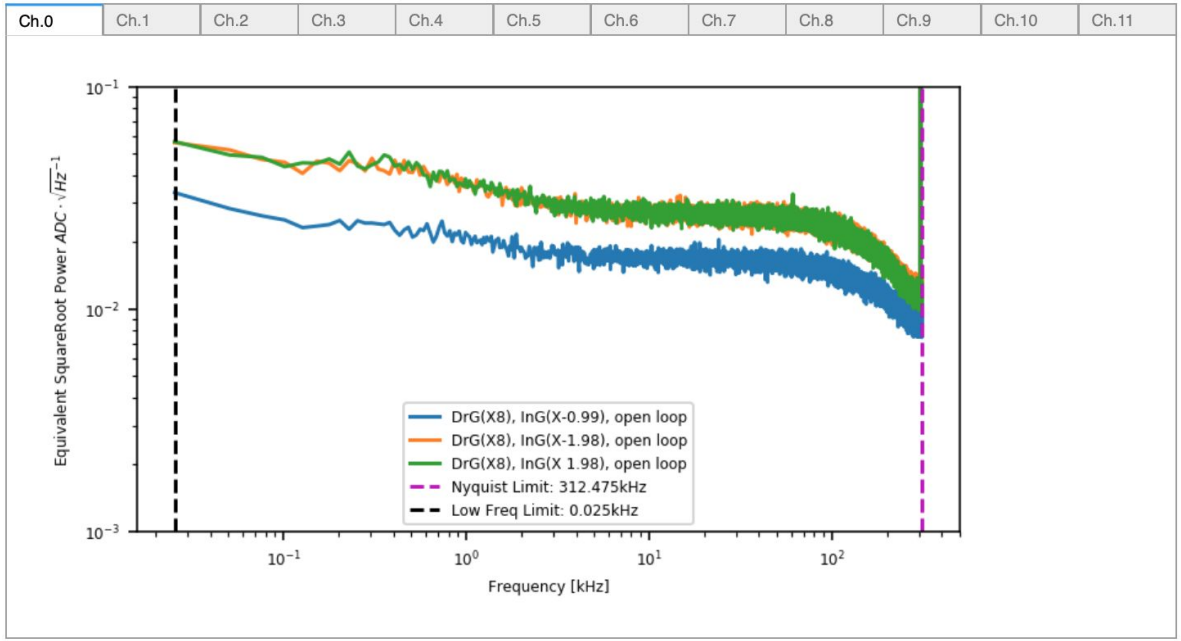


Back to 'Noise Test - PSD Evaluation'

7. Appendix 1.2, Typical Phonon PSDs, Pre/Post InG.

Board: SN49, tested on Sep 3, 20120.
Setting:

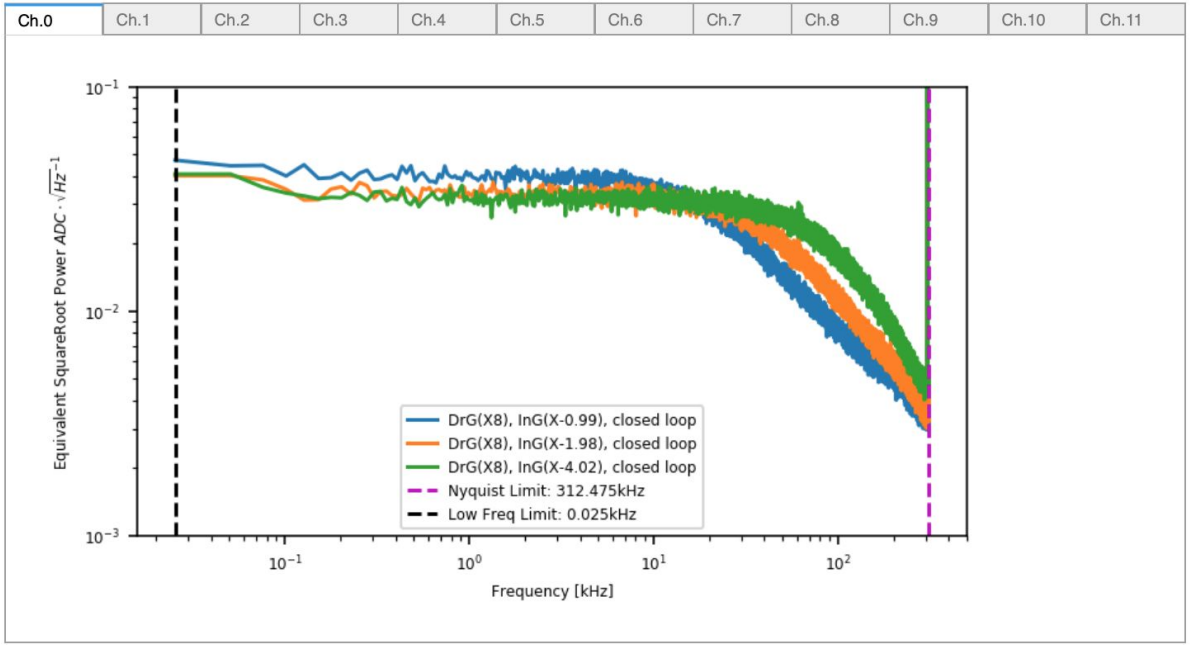
Src: PreAmp Mode.
DrG: 3(X8).
InG: 0xea(X-0.99), 0xd5(X-1.98), 0x2a(X1.98)



7. Appendix 1.2, Typical Phonon PSDs, feedback mode.

Board: SN49, tested on Sep 3, 20120.
Setting:

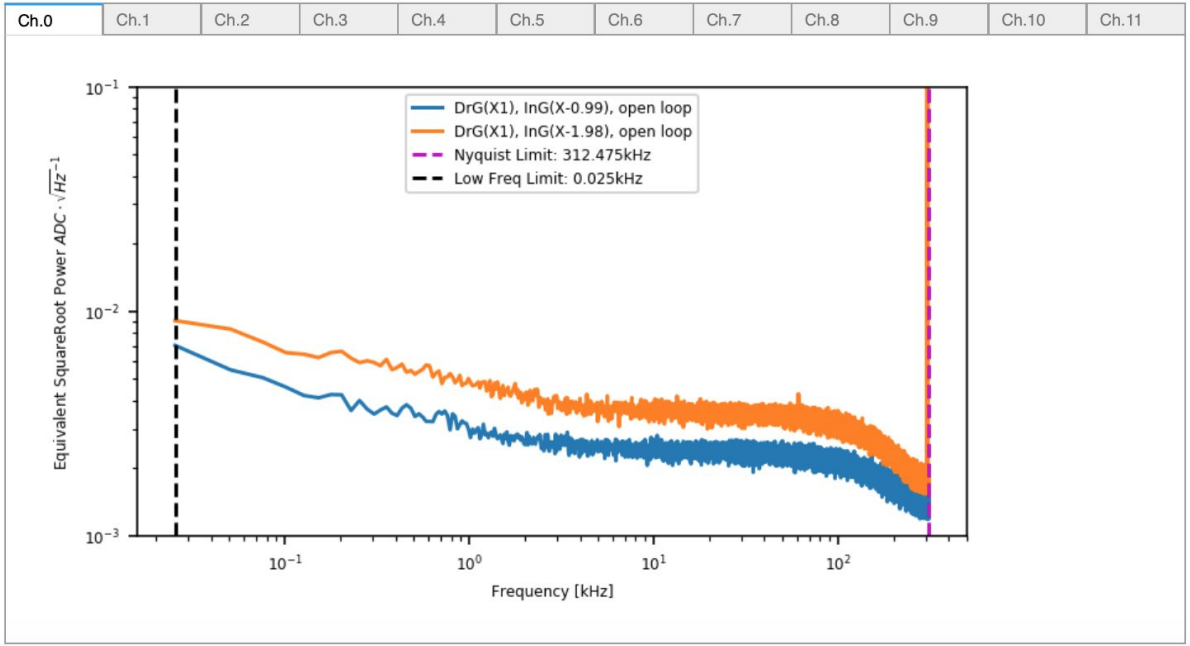
Src: Feedback/Closed mode.
DrG: 3(X8).
InG: 0xea(X-0.99), 0xd5(X-1.98), 0xaa(X-4.02)



7. Appendix 1.2, Typical Phonon PSDs, Small DrG noise

Board: SN49, tested on Sep 3, 20120.
Setting:

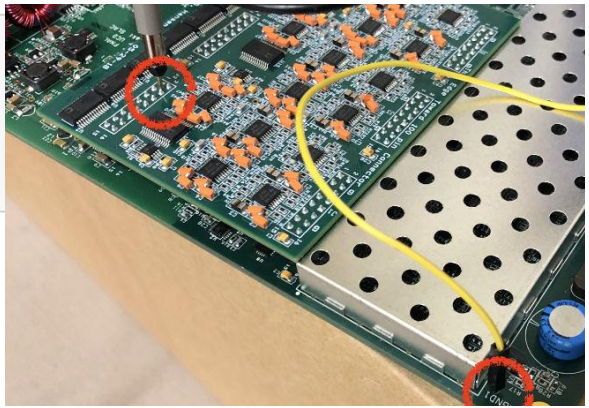
Src: PreAmp/Open Mode.
DrG: 0(X1).
InG: 0xea(X-0.99), 0xd5(X-1.98).



7. Appendix 2.0, more details about Calibration procedure

- Measure 13 points in (0x7000, 0x9000) for each register/pin:

```
%%time
points = 0x8000 + array([-0x1000, -0x800, -0x400, -0x100,
                         -0x80, -0x40, 0, 0x40, 0x80,
                         0x100, 0x400, 0x800, 0x1000])
DCRC.write_reg(pin_number, points[0])
time.sleep(5)
results = array([cal_point(pin_number, p, 5, DCRC, scope, offset_0) for p in points])
print("Done!")
```



- The code will automatically check the results are good or not, and then write the results (slope, slope_err, offset, offset_err, cov) into a txt file for each measurement if the results pass.

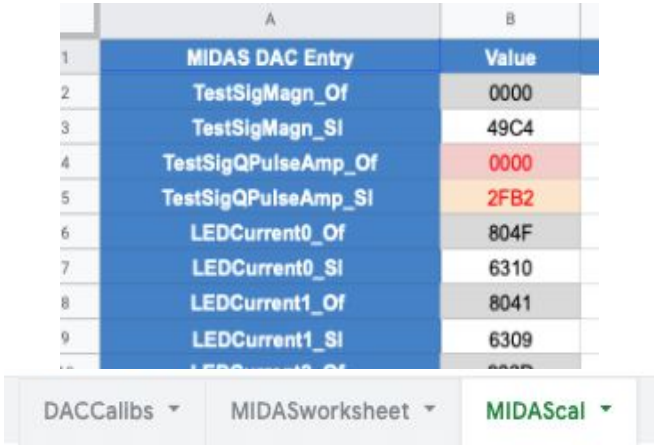
7. Appendix 2.0, more details about Calibration procedure

- Filling the results(slopes, offsets, their uncertainties) into the spreadsheet(template). See the spreadsheet template in TobackGroup's shared drive).

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q
DAC name (Midas)		DAC (ProjDefs)		Address	U-pin	J-pin	Slope/mV	S_error/mV	Offset/mV	O_error/mV	Corr_Coe	x(y=0) inter	RevE	RevD	RevD	Ground J pins
TestSignal Magnitude		DDSMagAddr		405	U147		1.888474	0.000106	-1.272396	0.069642	-0.7772504	0000				
				442												
ADCOffset	0	DrvOffset	0	760	16-1	J6-1	0.125018	0.0012595	-3.534608	0.343384	-1.37E-18	801C	1A	Phonon 2	DrvOfsA	J4-5, J4-12, J4-16
	1		1	761	16-7	J6-2	0.125559	0.0012595	3.746533	0.343384	-2.34E-19	7FE2	1B	Phonon 2	DrvOfsB	J4-5, J4-12, J4-16
	2		2	762	16-8	J6-3	0.12555	0.0012595	13.133545	3.97E-01	2.50E-10	7F97	1C	Phonon 2	DrvOfsC	J4-5, J4-12, J4-16
	3		3	763	16-14	J6-4	0.125499	0.0012595	14.366982	3.58E-01	1.25E-10	7F8D	1D	Phonon 2	DrvOfsD	J4-5, J4-12, J4-16
	4		4	764	8-1	J4-1	0.125056	0.0012595	20.838287	3.97E-01	2.50E-10	7F59	2A	Phonon 3	DrvOfsA	J2-5, J2-12, J2-16
	5		5	765	24-14	J4-2	0.125596	0.0012595	17.793451	3.97E-01	2.50E-10	7F72	2B	Phonon 1	DrvOfsD	J6-5, J6-12, J6-16
	6		6	766	24-1	J2-4	0.125348	0.0012595	35.139798	5.27E-01	5.00E-10	7EE7	3D	Phonon 1	DrvOfsA	J6-5, J6-12, J6-16
	7		7	767	24-7	J2-3	0.125445	0.0012595	13.748267	3.97E-01	2.50E-10	7F92	3C	Phonon 1	DrvOfsB	J6-5, J6-12, J6-16
	8		8	768	24-8	J2-2	0.125787	0.0012595	3.858032	3.43E-01	-9.41E-19	7FE1	3B	Phonon 1	DrvOfsC	J6-5, J6-12, J6-16
	9		9	769	8-8	J2-1	0.125976	0.0012595	20.475116	3.97E-01	2.50E-10	7F5D	3A	Phonon 3	DrvOfsC	J2-5, J2-12, J2-16
	10		10	76A	8-14	J4-4	0.125806	0.0012595	38.967418	5.27E-01	5.00E-10	7ECA	2D	Phonon 3	DrvOfsD	J2-5, J2-12, J2-16
	11		11	76B	8-7	J4-3	0.126038	0.0012595	15.092737	3.97E-01	2.50E-10	7F88	2C	Phonon 3	DrvOfsB	J2-5, J2-12, J2-16
	0		0	770	15-1	J5-6	0.125973	0.0012595	12.188894	0.397382	2.50E-10	7F9F	1A	Phonon 2	LPntA	J3-3, J3-13, J3-14
	1		1	771	15-7	J5-2	0.125525	0.0012595	4.848092	0.343383	-2.59E-18	7FD9	1B	Phonon 2	LPntB	J3-3, J3-13, J3-14
	2		2	772	10-7	J5-16	0.125122	0.0012595	8.828028	0.357648	1.25E-10	7FB9	1C	Phonon 2	LPntC	J3-3, J3-13, J3-14
	3		3	773	10-1	J5-12	0.125734	0.0012595	19.852166	0.397382	2.50E-10	7F62	1D	Phonon 2	LPntD	J3-3, J3-13, J3-14

7. Appendix 2.0, more details about Calibration procedure

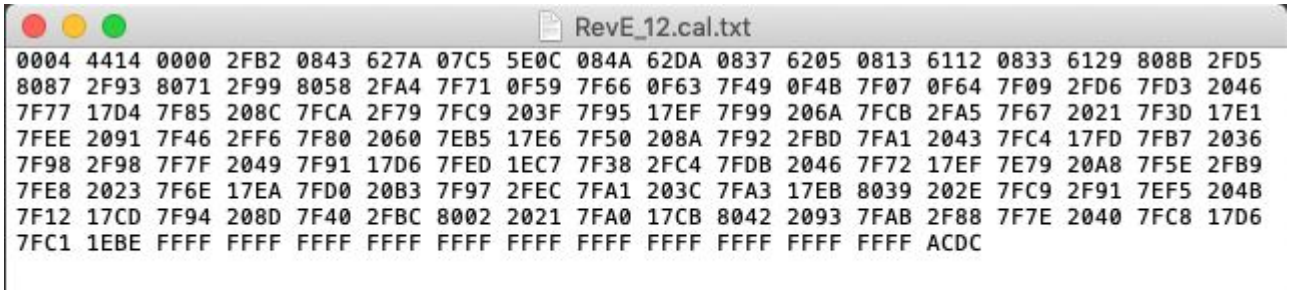
- Calibration parameters will be produced automatically in the 3rd sheet, **MIDAScal**. (number in red: default values, instead of measured ones)



	A	B
1	MIDAS DAC Entry	Value
2	TestSigMagn_Of	0000
3	TestSigMagn_SI	49C4
4	TestSigQPulseAmp_Of	0000
5	TestSigQPulseAmp_SI	2FB2
6	LEDCurrent0_Of	804F
7	LEDCurrent0_SI	6310
8	LEDCurrent1_Of	8041
9	LEDCurrent1_SI	6309

DACCalibs | MIDASworksheet | MIDAScal

- These values are calibration constants. Then we produce the midas file for each board, with proper format.

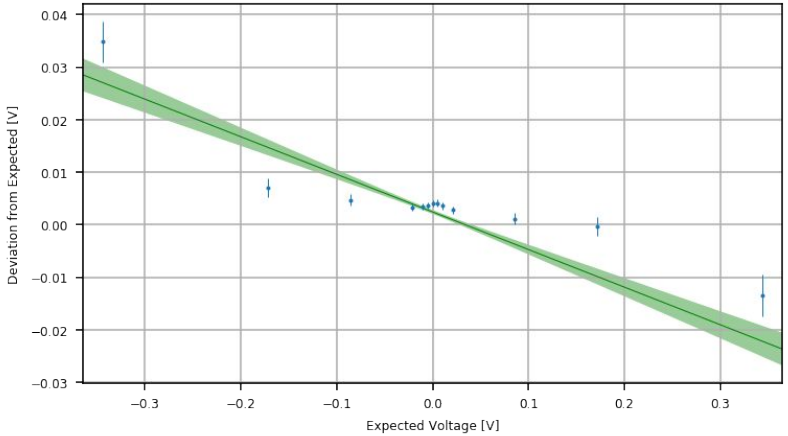


RevE_12.cal.txt

```
0004 4414 0000 2FB2 0843 627A 07C5 5E0C 084A 62DA 0837 6205 0813 6112 0833 6129 808B 2FD5
8087 2F93 8071 2F99 8058 2FA4 7F71 0F59 7F66 0F63 7F49 0F4B 7F07 0F64 7F09 2FD6 7FD3 2046
7F77 17D4 7F85 208C 7FCA 2F79 7FC9 203F 7F95 17EF 7F99 206A 7FCB 2FA5 7F67 2021 7F3D 17E1
7FEE 2091 7F46 2FF6 7F80 2060 7EB5 17E6 7F50 208A 7F92 2FBD 7FA1 2043 7FC4 17FD 7FB7 2036
7F98 2F98 7F7F 2049 7F91 17D6 7FED 1EC7 7F38 2FC4 7FDB 2046 7F72 17EF 7E79 20A8 7F5E 2FB9
7FE8 2023 7F6E 17EA 7FD0 20B3 7F97 2FEC 7FA1 203C 7FA3 17EB 8039 202E 7FC9 2F91 7EF5 204B
7F12 17CD 7F94 208D 7F40 2FBC 8002 2021 7FA0 17CB 8042 2093 7FAB 2F88 7F7E 2040 7FC8 17D6
7FC1 1EBE FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF ACDC
```

7. Appendix 2.1, example of BAD measurement in calibration

Deviation vs Expected Voltage Plot



Observed Voltage vs Expected Plot